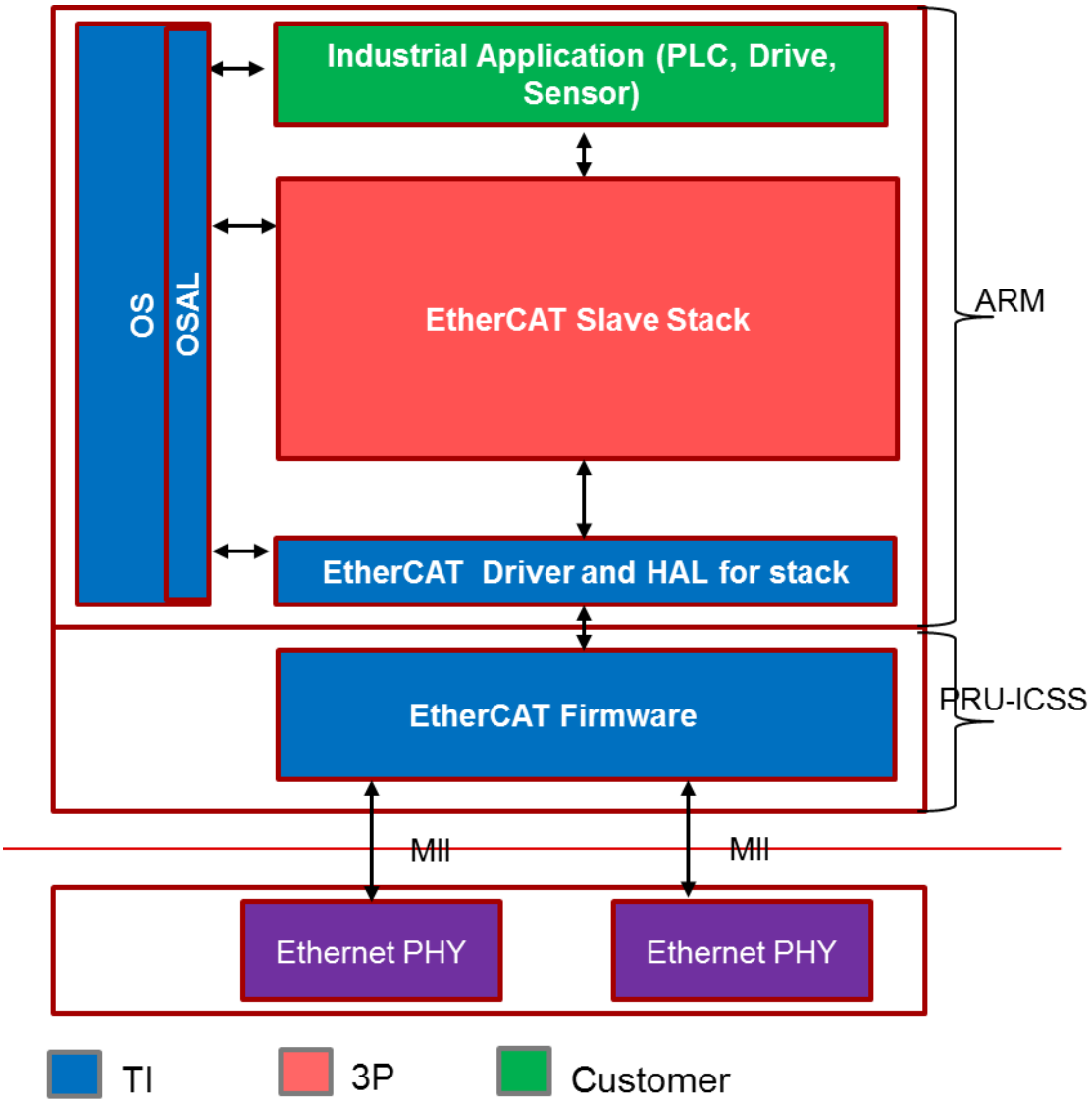
PRU-ICSS EtherCAT Slave Firmware Data Sheet

FEATURES

- All EtherCAT Commands (NOP, APRD, APWR, APRW, FPRD, FPWR, FPRW, BRD, BWR, BRW, LRD, LWR, LRW, ARMW and FRMW)
- 8 FMMU support
- 8 SM support
- 8KB(AM335, AMIC110) /28KB (AMIC120, AM437, AM57) /59KB (AM65x, AM64x) of Process Data RAM
- Distributed clocks (DC)
  - 64-bit DC
  - SYNC0 out generation single shot and cyclic mode support
  - SYNC1 out generation - SYNC1 cycle time multiple of SYNC0 cycle time
  - Latch0 and Latch1 inputs
  - System Time PDI control
- DL Loop Control
  - Using MII_RX_LINK (fast - depending on PHY link loss detection latency) – mandatory for cable redundancy support
  - Using PRU-ICSS MDIO state machine – not recommended for cable redundancy support
- Interrupts – AL and ECAT events
  - SYNC0, SYNC1 and PDI interrupt events on external SOC pins
- Watchdog – PDI and SM
- Error Counters
  - RX Invalid Frame Counter Port 0/1
  - RX ERR Counter Port 0/1
  - Forwarded Error Counter Port 0/1
  - ECAT Processing Unit Error Counter
- LED – Run, Error and Port0/1 activity based on firmware feedback
  - Controlled via GPIO from Host CPU based on firmware feedback or by PHY directly
- EEPROM Emulation for ESI EPPROM support
  - External flash for non-volatile storage support
- Management Interface for PHY over EtherCAT
- PHY address configuration and host side PRU-ICSS MDIO API for PHY programming
- Cable Redundancy support
- TI-ESC SPI Slave mode support (based on ET1100 protocol)
- On-chip memory execution support (without DDR)
- Enhanced Process Data Interface with EDMA support
- CiA402 Drive profile based Single-chip motor control support
- Reset isolation support on AM64x

Description

PRU-ICSS EtherCAT Software from TI can be used by customers to add EtherCAT function on top of Processor SDK to Sitara processors .PRU-ICSS EtherCAT firmware implements EtherCAT slave controller layer2 functionality with two MII ports (one IN and one OUT port per PRU-ICSS) in accordance with ETG1000 specification [5].This provides EtherCAT slave ASIC like functionality integrated into Sitara Processors with PRU-ICSS IP.



EtherCAT firmware for PRU-ICSS is a black box product maintained by TI. EtherCAT driver allows loading and running the EtherCAT firmware and acts as an interface with ESC firmware. This also includes PDI/Hardware abstraction layer (HAL) for popular EtherCAT stacks. EtherCAT driver is provided in full source so that customers can adapt this implementation to own hardware and Operating Systems.

EtherCAT Slave Stack typically consists of PDI/HAL, EtherCAT stack and user application which can be

customized. The behavior of the generic EtherCAT stack is described in ETG.1000 Specification [6]. Key components are EtherCAT state machine, real time Process Data Interface and Mailbox interface which provides non-real time interfaces like (AoE, CoE, EoE, FoE and SoE).

Performance Benchmarking : Cycle Time

The application was benchmarked for performance to figure out the lowest cycle time with which a given board can function. Benchmarking was done with 3 Boards running full mode application connected with Distributed Clocks (SYNC0) enabled and CoE data in “Auto-update” for all Objects. TwinCAT Master was used as the EtherCAT master for these tests. Below data is the lowest tested cycle time, cycle time lower that this might be possible depending on the loading and CPU operational frequency.

SOC/Board	ARM CPU Frequency	Lowest Cycle time (tested)	Remarks
AMIC11x / iceAMIC110	300 MHz	62.5 us	Tested in DC mode with CoE update enabled
AM335x / AM335x ICEv2	600 MHz	62.5 us	Tested in DC mode with CoE update enabled
AM437x / AM437x IDK	600 MHz	50 us	Tested in DC mode with CoE update enabled
AM57xx / AM57xx IDK	1 GHz	31.25 us	Tested in DC mode with CoE update enabled
AM65xx / AM65xx IDK	800 MHz	31.25 us	Tested in DC mode with CoE update enabled
AM64x	800 MHz	50 us	Tested in DC mode

Performance Benchmarking : Interrupt Processing Time

The application was benchmarked for performance to figure out the interrupt processing time for PDI and Sync ISRs. Benchmarking was done with 1 board running full mode application connected with Distributed Clocks (SYNC0) enabled. TwinCAT Master was used as the EtherCAT master for these tests. The cycle time was 50 us. Below data is the maximum time taken for PDI ISR and Sync ISR processing.

SOC/Board	ARM CPU Frequency	Cycle Time	PDI ISR Processing Time	Sync ISR Processing Time
AM64x	800 MHz	50 us	7.860 us	9.120 us

Performance Benchmarking : DC SYNC Jitter

The application was benchmarked for performance to figure out the worst case SYNC pulse jitter observed when boards are connected with Distributed Clock (SYNC0) enabled. The readings were taken with Boards running at 100us Cycle time (10000 packets/sec).

No.	Board Topology	Highest SYNC Pulse Jitter
1	TwinCAT Master <-> AM335x ICE <-> AM335x ICE	**13.2 ns**

Topology (1) oscilloscope capture showing Sync Pulse jitter measurement between two AM335x ICE boards

Performance Benchmarking : Enhanced Process Data Interface with EDMA Results

Read and write access latency for sync manager buffers in Process Data was measure for this benchmarking. The below improvements are measured using the maximum access latency recorded on AM437x IDK.

Process Data action	Max time in legacy application	Max time in Enhanced application	Improvement	Buffer Location
Read 253 bytes	25.4 µs	3.8 µs	**6.5x**	DDR (cached)
Write 263 bytes	6.7 µs	1.9 µs	**3.5x**	onChip RAM (non-Cached)
Read 5 bytes	1.9 µs	1.2 µs	**1.5x**	onChip RAM (non-Cached)
Write 7 bytes	2.4 µs	0.7 µs	**3x**	onChip RAM (non-Cached)

Performance Summary

A 300 MHz CPU speed is sufficient to support a simple IO or sensor application. More complex applications can use higher speed grades of up to 1.5 GHz depending on the SoC. The PRU core speed remains 200 MHz for all speed grades. AM572x IDK running default EtherCAT application (5 bytes output and 7 bytes input) on Cortex-A15 at nominal OPP (1GHz) can communicate with PLC at cycle time as low as 31.25 µs with Distributed Clocks (SYNC0) enabled

Memory Summary

This section describes memory usage of the EtherCAT PRU-ICSS firmware

Table 1 EtherCAT PRU-ICSS Firmware Memory Statistics

Memory	AM335x/AMIC110	AM437x/AM57xx	AM65xx/AM64x	Remarks
PRU-ICSS Shared RAM	12 KB	32 KB	63 KB	4KB Register memory and 8KB/28KB/59KB Process Data memory

Hardware Requirements

- Sitara Processor with PRU-ICSS IP and EtherCAT support
- ESC implementation uses following interrupts mapped to Host Interrupt Controller say GIC

Stack/application interrupts		
ESC firmware interrupt	**Host Interrupt**	**Remarks**
DC SYNC0 OUT	PRU_ICSS_EVTOUT1	Used in DC mode for syncing the application
DC SYNC1 OUT	PRU_ICSS_EVTOUT2	Used in DC mode for syncing the application
PDI Interrupt	PRU_ICSS_EVTOUT3	AL event/PDI interrupt to host stack
ESC command ACK	PRU_ICSS_EVTOUT4	ESC firmware command completion ACK to Host

- ESC implementation makes use of one instance of HW spinlock (SPINLOCK_LOCK_REG0)
- HW signals required to implement EtherCAT slave functionality is shown below, this info needs to be used in conjunction with http://www.ti.com/tool/PINMUXTOOL

NOTE: w.r.t prX, X is 1 or 2 (respectively PRU-ICSS1 or PRU-ICSS2 – refer to SOC TRM for availability)

Table 2 PRU-ICSS signals required for EtherCAT functionality

Signal name		Description
PRU-ICSS MDIO		
prX_mdio_mdclk	Mandatory	MDIO clock
prX_mdio_data	Mandatory	MDIO data
PRU-ICSS MII PORT0 (IN PORT) and PRU-ICSS MII PORT1 (OUT PORT)		
prX_mii_mt0_clk	Mandatory	MII0 and MII1 transmit clock
prX_mii_mt1_clk		
prX_mii0_txd3	Mandatory	MII0 and MII1 transmit data3
prX_mii1_txd3		
prX_mii0_txd2	Mandatory	MII0 and MII1 transmit data2
prX_mii1_txd2		
prX_mii0_txd1	Mandatory	MII0 and MII1 transmit data1
prX_mii1_txd1		
prX_mii0_txd0	Mandatory	MII0 and MII1 transmit data0
prX_mii1_txd0		
prX_mii0_rxd3	Mandatory	MII0 and MII1 receive data3
prX_mii1_rxd3		
prX_mii0_rxd2	Mandatory	MII0 and MII1 receive data2
prX_mii1_rxd2		
prX_mii0_rxd1	Mandatory	MII0 and MII1 receive data1

prX_mii1_rxd1		
prX_mii0_rxd0	Mandatory	MII0 and MII1 receive data0
prX_mii1_rxd0		
prX_mii0_txen	Mandatory	MII0 and MII1 TX enable
prX_mii1_txen		
prX_mii_mr0_clk	Mandatory	MII0 and MII1 receive clock
prX_mii_mr1_clk		
prX_mii0_rxdv	Mandatory	MII0 and MII1 RX data valid
prX_mii1_rxdv		
prX_mii0_rxer	Mandatory	MII0 and MII1 RXERR
prX_mii1_rxer		
prX_mii0_rxlink	Recommended	Enhanced link detection**/Redundancy support - connect LED_LINK/LED_SPEED from PHY here
prX_mii1_rxlink		
PRU-ICSS Distributed Clocks (Network clock synchronization)		
prX_edc_sync0_out	Recommended (for DC capable slaves)	SYNC0 out - Time synchronized OUT0
prX_edc_sync1_out	Optional	SYNC1 out - Time synchronized OUT1 (depends on SYNC0)
prX_edc_latch0_in	Optional	LATCH0 in (Time stamp latch input0)
prX_edc_latch1_in	Optional	LATCH1 in (Time stamp latch input1)
PRU-ICSS PDI Interrupt		
prX_edio_data_out0	Optional	PDI ISR output to external SOC pin (via one of the 8 PRU-ICSS digio outputs. PDI ISR pin can be selected via vendor specific register at offset 0xE0A.
prX_edio_data_out1		
prX_edio_data_out2		
prX_edio_data_out3		
prX_edio_data_out4		
prX_edio_data_out5		
prX_edio_data_out6		
prX_edio_data_out7		
ESC LED control*		
Any available GPIOs can be used for this purpose. Requires 4 LED_RUN (Green), LED_ERR(Red), LED_LINK/ACT0, LED_LINK/ACT0	Mandatory	RUN and ERR LED are controlled by stack. LED_LINK/ACT0/1 are controlled by Ethernet PHY.

*: Refer to ETG.1300 – Indicator and Labeling specification [7] and ETG.9001 – Marking Rules [8] to make sure that product conformance requirement are met

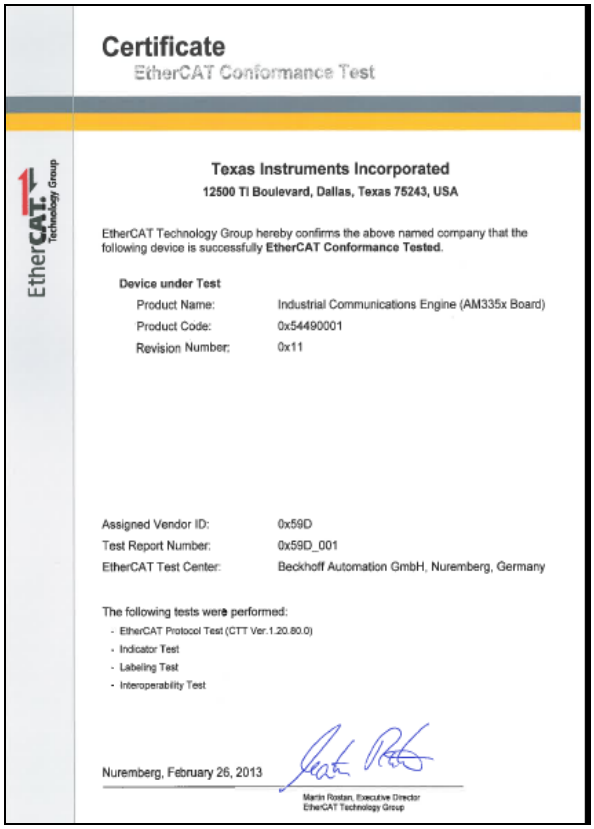
Software

EtherCAT slave firmware, driver, examples and associated documentation for Sitara Processors is available from http://www.ti.com/tool/PRU-ICSS-ETHERCAT-SLAVE. EtherCAT software runs on top of TI Processor SDK

More details are available in the below mentioned links
http://software-dl.ti.com/pru-icss-industrial-sw/esd/docs/indsw/index.html
http://software-dl.ti.com/processor-sdk-rtos/esd/docs/latest/rtos/index.html
http://software-dl.ti.com/processor-sdk-rtos/esd/docs/latest/linux/index.html

Certification Information

Certification was done on AM335x ICEv1 board using EtherCAT firmware build (1.2.42) and Beckhoff SSC 5.0.1 EtherCAT slave stack during Feb 2013



Certificate

EtherCAT Conformance Test

Texas Instruments Incorporated

12500 TI Boulevard, Dallas, Texas 75243, USA

EtherCAT Technology Group hereby confirms the above named company that the following device is successfully **EtherCAT Conformance Tested**.

Device under Test

Product Name:	Industrial Communications Engine (AM335x Board)
Product Code:	0x54490001
Revision Number:	0x11

Assigned Vendor ID:	0x59D
Test Report Number:	0x59D_001
EtherCAT Test Center:	Beckhoff Automation GmbH, Nuremberg, Germany

The following tests were performed:

- EtherCAT Protocol Test (CTT Ver.1.20.80.0)
- Indicator Test
- Labeling Test
- Interoperability Test

Nuremberg, February 26, 2013

Martin Rostan, Executive Director
EtherCAT Technology Group

References

1. EtherCAT on Sitara Processors - spry187e
2. Industrial Communications Solution Guide - slyy050b
3. EtherCAT Communications Development Platform
4. Single Chip Drive for Industrial Communications and Motor Control
5. ETG.1000 part 4 Data link Layer protocol specification
6. ETG.1000 part 6 Application link Layer protocol specification
7. ETG.1300 Indicator and Labelling specification
8. ETG.9001 Marking Rules
9. EtherCAT ESC datasheet Section I - Technology
10. EtherCAT ESC datasheet Section 2 - Register Description
11. http://processors.wiki.ti.com/index.php/PRU_ICSS_EtherCAT_firmware_API_guide#PRU-ICSS_EtherCAT_Register_List
12. Beckhoff SSC documentation available as part of ET9300 EtherCAT Slave Stack Code (http://www.ethercat.org/memberarea/stack_code.aspx)
13. EtherCAT Slave Implementation Guide from ETG
14. ESD EtherCAT Slave Stack : https://esd.eu/en/products/ethercat-slave
15. icECAT Linux SDK from ibv : http://www.ibv-augsburg.net/media/pdf/icECAT_Slave_SDK_Linux_Whitepaper.pdf

Acronyms

Acronym	Description
PRUSS	Programmable RealTime Unit Sub System
PRU-ICSS	Programmable RealTime Unit - Industrial Communication Sub System - PRUSS with industrial communication support
ESC	EtherCAT Slave Controller
ECAT	EtherCAT
PDI	Process Data Interface (Host interface to ESC)
FMMU	Fieldbus Memory Management Unit
SM	Sync Manager
SSC	Slave Stack Code (from Beckhoff)
DL	Datalink Layer
ESI	EtherCAT Slave Information
ISR	Interrupt Service Routine
AL	Application Layer
LED	Light Emitting Diode
HAL	Hardware Abstraction Layer
AoE	ADS over EtherCAT
CoE	CANopen application profile over EtherCAT
EoE	Ethernet over EtherCAT
FoE	File Transfer over EtherCAT
SoE	Servo drive profile over EtherCAT
PDO	Process Data Object
PLC	Programmable Logic Controller
HAL	Hardware Abstraction Layer
MDIO	Management Data Input Output
MII	Media Independent Interface
ASIC	Application Specific Integrated Circuit
OS	Operating Systems
SoC	System On Chip
IDK	Industrial Development Kit (EVM)

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